Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **1A**
2. **1Y**
3. **2A**
4. **2Y**
5. **3A**
6. **3Y**
7. **GND**
8. **4Y**
9. **4A**
10. **5Y**
11. **5A**
12. **6Y**
13. **6A**
14. **VCC**

**14**

**1**

**4**

**MASK**

**REF**

**L**

**S**

**1**

**2**

**3**

**4**

**5**

**6**

**13**

**12**

**11**

**10**

**9**

**8**

**7**

**.042”**

**.051”**

**Top Material: Al**

**Backside Material: Al**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: LS14**

**APPROVED BY: DK DIE SIZE .042” X .051” DATE: 4/19/21**

**MFG: TEXAS INSTRUMENTS THICKNESS .011” P/N: 54LS14**

**DG 10.1.2**

#### Rev B, 7/19/02